

# 28–36 GHz GaAs MMIC Low Noise Amplifier



AA035N1-00, AA035N2-00

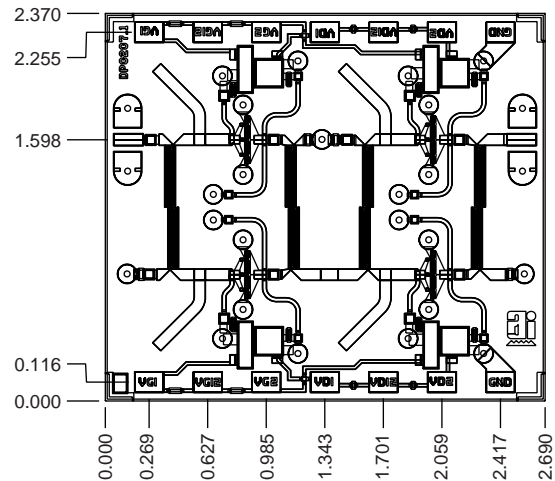
## Features

- Dual Bias Supply Operation (4.5 V)
- 2.8 dB Typical Noise Figure at 32 GHz
- 12 dB Typical Small Signal Gain
- 0.25  $\mu\text{m}$  Ti/Pd/Au Gates
- 100% On-Wafer RF, DC and Noise Figure Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

## Description

Alpha's two-stage balanced 28–36 GHz MMIC low noise amplifier has typical small signal gain of 12 dB with a typical noise figure of 2.6 dB at 32 GHz. The chip uses Alpha's proven 0.25  $\mu\text{m}$  low noise PHEMT technology, and is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate a conductive epoxy die attach process.

## Chip Outline



Dimensions indicated in mm.  
All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.  
Chip thickness = 0.1 mm.

## AA035N1-00 Electrical Specifications at 25°C ( $V_{DS} = 4.5\text{ V}$ , $I_D = 70\text{ mA}$ )

Parameter	Condition	Symbol	Min.	Typ. <sup>3</sup>	Max.	Unit
Drain Current		$I_{DS}$		70	90	mA
Small Signal Gain	F = 28–36 GHz	G	10	12		dB
Noise Figure	F = 32 GHz	NF		2.8	3.2	dB
Input Return Loss	F = 28–36 GHz	$RL_I$		-17	-12	dB
Output Return Loss	F = 28–36 GHz	$RL_O$		-20	-12	dB
Output Power at 1 dB Gain Compression <sup>1</sup>	F = 35 GHz	$P_1$ dB		10		dBm
Thermal Resistance <sup>2</sup>		$\theta_{JC}$		50		°C/W

## AA035N2-00 Electrical Specifications at 25°C ( $V_{DS} = 4.5\text{ V}$ , $I_D = 70\text{ mA}$ )

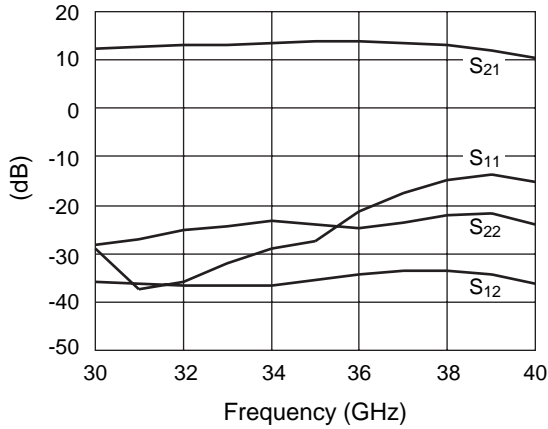
Parameter	Condition	Symbol	Min.	Typ. <sup>3</sup>	Max.	Unit
Drain Current		$I_{DS}$		70	90	mA
Small Signal Gain	F = 28–36 GHz	G	9	12		dB
Noise Figure	F = 32 GHz	NF		3.0	3.8	dB
Input Return Loss	F = 28–36 GHz	$RL_I$		-17	-12	dB
Output Return Loss	F = 28–36 GHz	$RL_O$		-20	-12	dB
Output Power at 1 dB Gain Compression <sup>1</sup>	F = 35 GHz	$P_1$ dB		10		dBm
Thermal Resistance <sup>2</sup>		$\theta_{JC}$		50		°C/W

1. Not measured on a 100% basis.

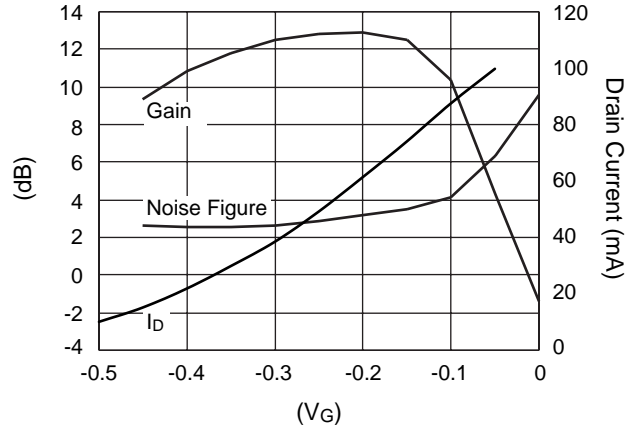
2. Calculated value based on measurement of discrete FET.

3. Typical represents the median parameter value across the specified frequency range for the median chip.

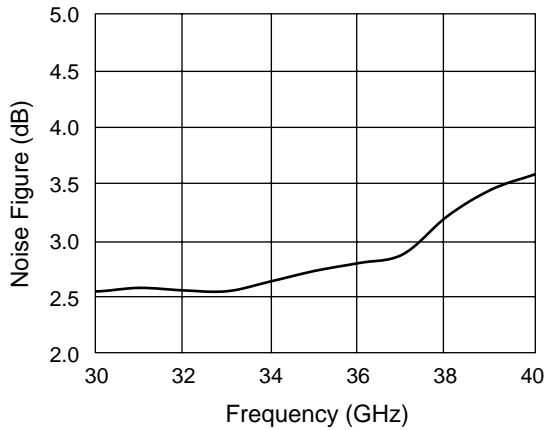
### Typical Performance Data



Typical Small Signal Performance S-Parameters ( $V_D = 4.5\text{ V}$ )



Typical 35 GHz Noise Figure and Gain as a Function of Gate Voltage ( $V_G$ )

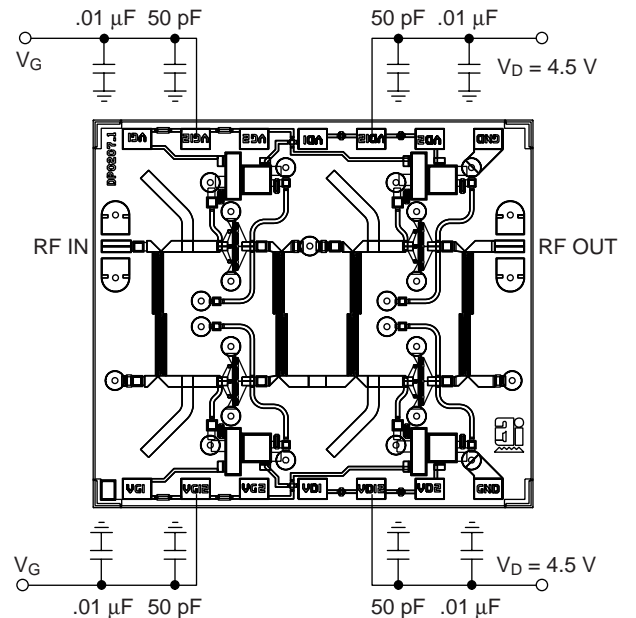


Typical Noise Figure Performance vs. Frequency

### Absolute Maximum Ratings

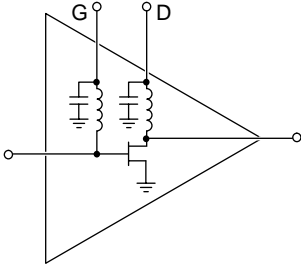
Characteristic	Value
Operating Temperature ( $T_C$ )	-55°C to +90°C
Storage Temperature ( $T_{ST}$ )	-65°C to +150°C
Bias Voltage ( $V_D$ )	5.5 $V_{DC}$
Power In ( $P_{IN}$ )	16 dBm
Junction Temperature ( $T_J$ )	175°C

### Bias Arrangement



For biasing on, adjust  $V_G$  from zero to the desired value (-0.3 V typically is optimum). Then adjust  $V_D$  from zero to the desired value (4.5 V recommended). For biasing off, reverse the biasing on procedure.

### Circuit Schematic



Detail A

